REMARKS

Claims 1-16 were presented for examination. By the aforementioned Office Action, Claims 6-9 and 11-16 were rejected under 35 USC § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 1 was rejected under 35 USC § 102 as being anticipated by Nakao (US 5,552,727) and also by Kuge (US 2001/0043102A1). Claim 10 was rejected under 35 USC § 103(a) as being obvious, and therefore unpatentable, over Nakao and also over Kuge.

By this response, Claim 1 has been cancelled, Claims 2 and 3 have been recast into independent claims by including the features of Claim 1, Claims 6-8 and 12 have been amended to more particularly and distinctly point out Applicant's invention, Claim 10 has been amended to indicate its correct dependency, and Claim 14 has been amended to correct a typographical error. Support for the amendments is found in the originally filed specification and drawings. No new matter is added. For the reasons set forth below, reconsideration is respectfully requested.

Rejection under 35 USC §112

The amended Claim 6 now recites the inputs of the 3-input AND gate in the order corresponding to the naming conventions of the signals received thereby. Specifically, the first input is recited to be coupled to a generated signal (IN1) that is recited in the amended Claim 5 wherein the generated signal (IN1) is the reference clock signal delayed substantially by 2Y, the second input is recited to be coupled to the reference clock signal (IN2) and the third input is recited to be coupled to the reference clock signal that is inverted and delayed by a known width Y (IN3) as shown in Figure 4. Claim 6 now conforms both to Figure 4 as well as Claim 5 which it depends from.

The amended Claim 7 now clarifies that the recited width Y-X is that of a pulse generated by the pulse generator, and that X is a phase difference between the reference clock signal and the output clock signal.

The amended Claim 8 now correctly recites that "the third (instead of second) input is coupled to the reference clock signal that is inverted and delayed by Y+D" as shown in Figure 4.

The amended Claim 12 now recites "the reference clock signal" in line 12-13. Therefore, it is now clarified that this reference clock signal is a delayed version of the reference clock signal recited in line 2 of Claim 12.

In view of the foregoing, it is submitted that Claims 6-9, 11-16 are now definite, and thus, allowable under 35 USC §112.

Allowable Subject Matter

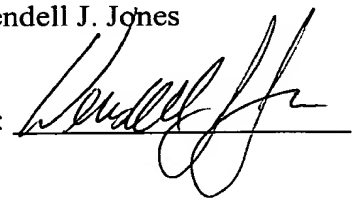
Claims 2 and 3 which have been recast in independent form including all features of Claim 1 are now allowable. Accordingly, since Claims 4-11 depend from either Claim 2 or Claim 3, Claims 4-11 are also allowable.

In view of the foregoing, it is respectfully submitted that the grounds for the Examiner's rejections have been overcome and Claims 2-16 should be found to be in condition for allowance.

Date: 12/29/2003

Respectfully submitted,

Wendell J. Jones

By: 

Hewlett Packard Company.
Intellectual Property Administration
P.O. Box 272400
3404 E. Harmony Road
Fort Collins, CO 80527-2400